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Self-organized quantum dots for future semiconductor memories

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Abstract
A memory structure based on self-organized quantum dots (QDs) combining the advantages of dynamic random access memory (DRAM) and flash memory which enables extremely fast write times (<1 ns) together with long storage times ($\gg$10 years) at room temperature is presented. A storage time of 1.6 s at 300 K in InAs/GaAs QDs with an additional $Al_{0.9}Ga_{0.1}As$ barrier—100 times longer than in a DRAM—is demonstrated. Much longer retention times of 10^6 years are predicted for GaSb QDs in an AlAs matrix. A minimum write time of 6 ns is currently obtained for InAs/GaAs QDs, of the order of those for present DRAMs. An even faster write time below 1 ns, only limited by charge carrier capture and relaxation times (in the order of picoseconds), is predicted for a slightly improved device structure.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Mainly just two different semiconductor memories dominate today's electronic devices: the dynamic random access memory (DRAM) [1] and the flash memory [2, 3]. The DRAM is used as the main memory in personal computers, where fast access times (<20 ns) in combination with a good endurance (>10^{15} write/erase cycles) is needed. However, the DRAM is a volatile memory with large power consumption, as the information has to be refreshed within tens of milliseconds. The flash memory is a nonvolatile memory having an retention time of more than 10 years without power consumption; hence it is mainly used in mobile phones, MP3 players, digital cameras, etc. In a flash memory, a floating gate in a metal oxide semiconductor field effect transistor (MOSFET) acts as the storage unit, while surrounding SiO_2 barriers with an energetic height of 3.2 eV maintain the nonvolatility. These barriers, however, lead to a poor write time (microseconds) and endurance (<10^6), since hot electrons have to be injected into the gate, destroying it in the long run. Future nonvolatile memories should show better endurance and faster write/read time, equal to or better than those of a DRAM. Phase change memories, ferroelectric or magnetic random access memories [4] are thought to present alternatives, but do not yet provide the desired high write speed.

One of the promising options is the use of self-organized materials in future memory devices, especially quantum dots (QDs) [5, 6] based on III–V materials. Using these nano-objects in a floating gate structure would have lots of advantages as compared to silicon based structures. QDs can be fabricated by a 'bottom-up approach', e.g., in a Stranski–Krastanov growth mode, where small islands are formed by self-organization without lithography. A variety of material combinations allow band structure engineering with tunable band offsets and barriers, in contrast to the fixed SiO_2 barriers in modern flash memories. Memories based on III–V material may overcome the flash problems [7] and produce a nonvolatile memory which has better endurance and a fast access time below 1 ns, faster than that of a DRAM cell.

In this paper, we present a memory concept based on QDs, which should enable very fast write times (<ns) shorter than for DRAM and independent of the carrier storage time, e.g., in combination also with a storage time ($\gg$10 years), longer than in a flash. The write time in our concept is limited only by the charge carrier relaxation time, from the band edge into the QD states, which is below picoseconds at room temperature [8, 9], more than four orders of magnitude faster than the write time of a DRAM cell. We show for InAs QDs with an $Al_{0.9}Ga_{0.1}As$ barrier a storage time of seconds at room

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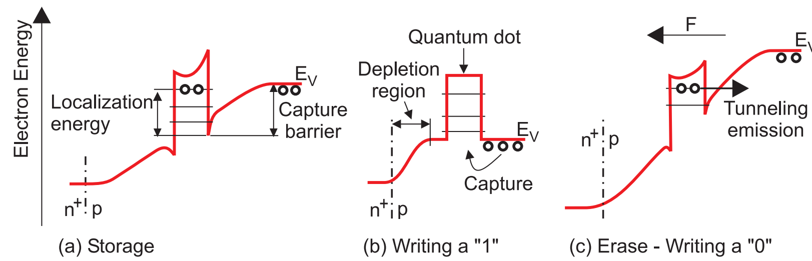

Figure 1. Schematic illustration of the storage (a), write (b), and erase (c) process in the proposed QD based flash memory based on hole storage.

temperature and propose more than 10^6 years for GaSb QDs in an AlAs matrix [10]. We present a minimum write time of 6 ns in InAs/GaAs QDs, already in the order of the present access time of a DRAM cell [11]. The write time is at the moment limited by the RC low pass of the device and can be easily reduced.

2. Operation principle of a QD memory

In a conventional flash memory, a Si based floating gate placed between two SiO_2 barriers stores the charge carriers. The SiO_2 barriers have the enormous energetic height of 3.2 eV, essential for storing carriers for more than 10 years at room temperature. The barrier height is fixed, and during the write process the floating gate has to be charged with electrons by Fowler–Nordheim tunneling and/or hot-electron injection. Both charging mechanisms cause the two main disadvantages of a flash cell: the slow write time in the order of microseconds and the poor endurance in the order of 10^6 write/erase cycles.

Our concept of a QD based memory eliminates the drawbacks of the 'fixed height' of SiO_2 barriers by using a tunable barrier height which can be decreased during the write operation. In addition, using III–V compound semiconductors allows band structure engineering with an *adjustable* localization energy which determines the charge carrier storage time [12, 10]. Thus our concept consists of three parts. First, the QDs are used as storage units for the charge carriers. Second, the QDs are placed inside a p–n or p–i–n diode structure, near to or inside the depletion region. By modifying the depletion region the memory operations—storage, writing and erasing—are realized. Third, the read operation is realized by placing a two-dimensional electron gas (2DEG) below the QD layer, like in a conventional flash cell [4]. This principle was already demonstrated for the read-out process in a QD based memory by Balocco *et al* [13].

The charge carrier storage and the write/erase operations work as follows (schematically depicted in figure 1): at zero bias, the doping concentration and the location of the QDs in the structure are adjusted such that the QDs are inside the depletion region. This represents the storage situation; figure 1(a). The width of the depletion region can be changed by an applied external bias. A forward bias reduces the width and the QDs are outside the depletion region; figure 1(b). Hence, in contrast to the flash memory concept with the fixed SiO_2 barrier height, the capture barrier is eliminated and very fast capture into the QD states is possible. To erase the information, a high reverse bias is applied to the diode; figure 1(c). The QDs are inside the depletion region with a strong electric field enabling tunneling of the charge carriers through the triangular barrier.

3. Storage time at room temperature

A first milestone for using QDs as storage units is demonstrating a storage time in the order of milliseconds, the crucial DRAM refresh time. As the storage time in QDs depends on the localization energy of the charge carriers, material combinations with a large band offset between QD and matrix are promising. We have previously determined storage times and localization energies of holes in a number of QD material systems [10, 14, 15, 12, 16] using deep level transient spectroscopy (DLTS) [17]. An increase in the hole storage time at room temperature by more than nine orders of magnitude from nanoseconds up to seconds was observed as the hole localization energy increased from 210 meV in InAs/GaAs QDs up to 710 meV in InAs/GaAs QDs with an additional $Al_{0.9}Ga_{0.1}As$ barrier. This localization energy leads to a hole storage time of about 1.6 s at room temperature, three orders of magnitude longer than the crucial DRAM refresh time [10]. We are able to determine directly this hole storage time. In charge-selective DLTS experiments the QDs are situated inside the depletion region of the p–n diode and the depletion capacitance depends on the charge carrier population in the QDs. It follows that the charge carrier emission from the QD ground state of the QD ensemble recorded as a capacitance transient, shown in figure 2, represents the decrease in the hole population of the ground state of the QD ensemble. This transient measured at 300 K is shown in figure 2 and shows a mono-exponential decay with a time constant of 1.6 s.

The hole storage time is plotted versus the localization energy for different III–V self-organized QDs in figure 3, as solid dots. The storage time shows an exponential dependence on the localization energy as predicted by the common rate equation of thermally activated emission [17]. It increases by one order of magnitude for an increase in the localization energy of about 50 meV. From the experimental results a hole localization energy can be estimated, which provides a storage time of 24 h/10 years. These storage times are reached for localization energies of 0.96 eV and 1.14 eV, respectively.

We calculated the hole localization energies for different antimony based QDs using eight-band $k \cdot p$ theory [10, 18]

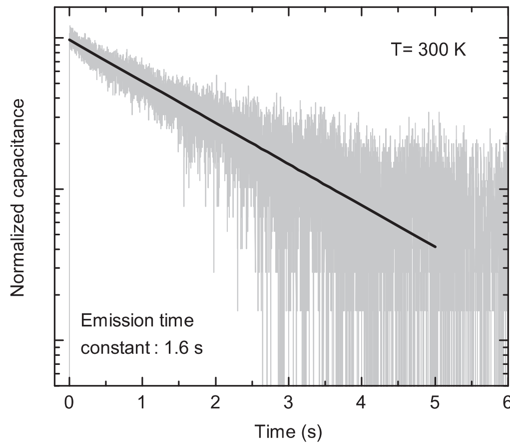

Figure 2. A capacitance transient at 300 K for hole emission from the ground state of the QD ensemble. The black solid line is a mono-exponential fit yielding a time constant of 1.6 s.

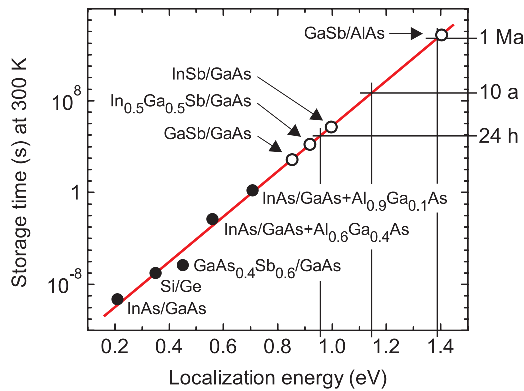

Figure 3. Hole storage time versus the localization energy for different QD systems. The solid line is a fit to the experimental data (full circles). The open circles are predicted storage times.

to estimate the hole storage time at room temperature. The calculated values are plotted in figure 3, as open circles. A hole storage time in InSb/GaAs QDs of more than 24 h is predicted (see figure 3). Using an $Al_xGa_{1-x}As$ instead of a GaAs matrix, a storage time of more than 10 years can be achieved. Since the valence band offset between GaAs and AlAs is about 550 meV [19] the entire hole localization energy in GaSb/AlAs QDs is about 1.4 eV. This value could lead to an average hole storage time of more than one million years at room temperature (see figure 3), orders of magnitude longer than needed for a nonvolatile memory. Therefore, on the basis of the experimental results, type II (In)(Ga)Sb QDs in a Al(Ga)As matrix are considered to provide a very promising material combination for a future nonvolatile QD memory.

4. Fast write time in a QD memory

To prove the potential of the memory concept, we have investigated the write process in QD based memory structures. Two samples were investigated containing type I InAs/GaAs and type II GaSb/GaAs QDs in an n^+–p diode [11]. This allows us to measure the write times in two different devices

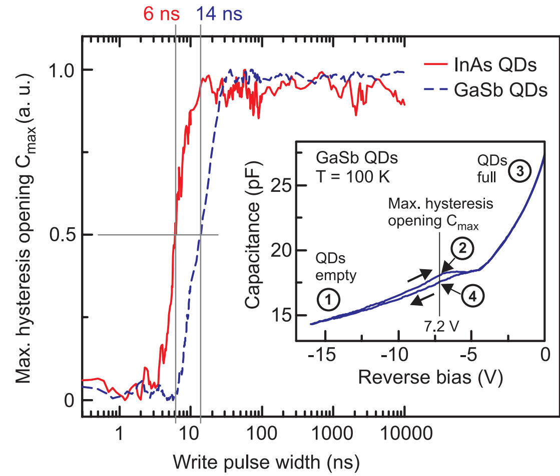

Figure 4. Maximum hysteresis opening C_{max} for different write pulse widths. The inset shows the capacitance sweep of a n^+–p diode containing GaSb/GaAs QDs.

storing holes. The charge states of the QDs were read out by measuring the capacitance of the n^+–p diode. A larger capacitance corresponds to unoccupied QDs (‘0’), while a smaller capacitance represents a ‘1’, where the QDs are filled with holes.

The inset in figure 4 shows the switching between the two states, by means of a hysteresis curve of the capacitance for the GaSb/GaAs QD sample. At the reverse bias of 16 V (point 1) the charge carriers tunnel out of the QDs (erase the information). If the reverse bias is now swept from 16 V to the storage situation at 8.2 V (InAs QDs) or 7.2 V (GaSb QDs), the QDs are empty and a larger capacitance is observed (point 2). If the bias is swept to 0 V (point 3), the QDs are charged with holes and a smaller capacitance is observed upon sweeping back to the storage situation (point 4). The maximum hysteresis opening is now defined at the storage position as the difference between the capacitance values for a ‘0’ and for a ‘1’ state.

To study the limit of the write time, series of write pulses were applied with decreasing pulse widths down to 300 ps. The cycle started with a 10 s long erase pulse at $V_r = 16$ V (point 1 in the inset of figure 4). Then the capacitance of the device structure was measured at the storage position (point 2) at 7.2 V (GaSb QDs) and 8.2 V (InAs QDs). A write pulse of $V_r = 0$ V was applied to the device (point 3) and the capacitance was again measured at the storage situation point 4. The maximum hysteresis opening C_{max} is plotted versus the write pulse width in figure 4. The limit of the write time is reached when the QDs are not sufficiently charged any longer. The hysteresis opening C_{max} vanishes and we define the limit as a drop in C_{max} to 50%.

Minimum write times of 6 ns at $T = 25$ K for the InAs QD sample and 14 ns at $T = 100$ K for the GaSb QD sample are obtained. These values are already in the order of the write time in a DRAM cell. The measured write time is at the moment limited by the experimental set-up and the parasitic cut-off frequency of the RC low pass of the devices. This assumption is also confirmed by previous measurements [9] of the same structure, where average hole capture and relaxation

times were found of the order of picoseconds. The difference between the write times is due to a slightly different *RC* low passes of the two samples. Much faster write times below 1 ns are feasible for improved memory structures having higher external cut-off frequencies.

5. Conclusion

In conclusion, we have presented a memory concept based on self-organized QDs, enabling very fast write times in combination with long storage times. The physical limitation of the write time in such a QD based memory is given by the relaxation time of the charge carriers, known to be in the picosecond range. We have investigated the performance of QD memory structures in terms of write and storage time. We have measured an average storage time of holes in InAs/GaAs QDs with an additional $Al_{0.9}Ga_{0.1}As$ barrier of 1.6 s at room temperature and predicted a retention time of about 10^6 years for GaSb QDs in an AlAs matrix. We have demonstrated a write time of 14 ns in GaSb/GaAs QDs and 6 ns for InAs/GaAs QDs. These write times are at the moment simply limited by the parasitic cut-off frequency of the *RC* low pass of the devices. Faster write times below 1 ns are expected for improved device structures.

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